REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1, 4, 7, and 14 have been amended as set forth herein.

Claims 1-20 remain pending in this application.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTION UNDER 35 U.S.C. § 103

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,563,837 to *Krishna, et al.*, hereinafter "Krishna". The Applicant respectfully traverses the rejection.

In rejecting claims under 35 U.S.C. § 103(a), the examiner bears the initial burden of establishing a *prima facie* case of obviousness. (*In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). See also *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984)). It is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. (*Id.* at 1073, 5 USPQ2d at 1598). In so doing, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), *viz.*, (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; and (3) the level of ordinary skill in the art. In addition to these

factual determinations, the examiner must also provide "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir 2006) (cited with approval in *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007)).

Claim 1 comprises unique and novel elements, including those emphasized below:

> 1. For use in a fixed-size packet switch, a switch fabric comprising:
>
> N input buffers to receive incoming fixed-size data packets from an input port at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate, wherein said N input buffers are internal to said switch fabric and are external to said input port;
>
> N output buffers to receive fixed-size data packets at said second data rate and to output said fixed-size data packets to an output port at said first data rate, wherein said N output buffers are internal to said switch fabric and are external to said output port; and
>
> *a bufferless, non-blocking interconnecting network to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate; and*
>
> a scheduling controller connected to the bufferless, non-blocking interconnecting network, *wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network.* [Emphasis Added]

Claim 1 has been amended to include the element " wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network." This element is fully support by the specification, including paragraph [0033] and [0034], which are reproduced below:

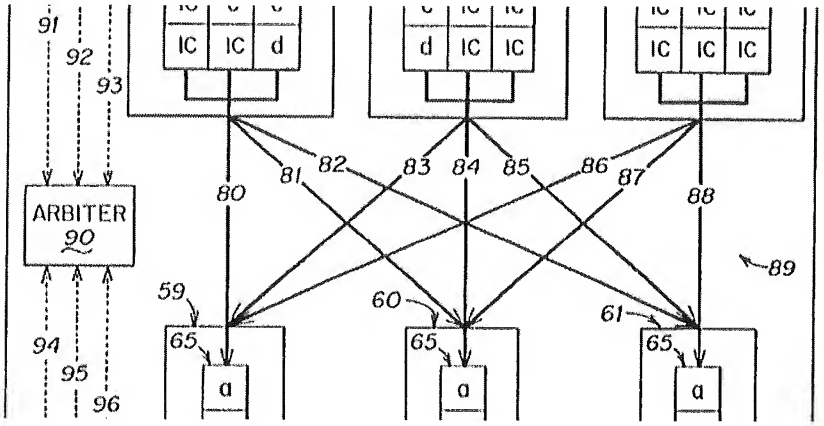
[0033] Scheduling by scheduling controller 240 consists of two tasks: 1) scheduling the forwarding of cells from the N external input buffers (i.e., input ports 210) to the internal input buffers (i.e., input buffers 321-323); and (2) scheduling the switching of cells in internal input buffers 321-323 to internal output buffers 331-333. In principle, the CIOQ is controlled by the scheduling controller 240 to simulate an internally buffered crossbar (IBX). It is not required to be an exact simulation, but the delay discrepancy is tightly upper bounded by 2N slots. This can be done because, in a VOQ+IBX switch, there are at most T cells transmitted or received by an input or output port over any time interval of T slots.

[0034] FIG. 4 depicts flow chart 400, which illustrates the operation of exemplary packet switch 111 according to one embodiment of the present invention. During input scheduling, a cell is forwarded to the corresponding one of internal input buffers 321-323 if it would be forwarded to the an internally buffered crossbar (IBX) in the simulated switch (process step 405). During output scheduling, each cell is marked at its internal input buffer in the CIOQ as being active if it is selected by its destined output in the simulated switch to be transmitted out (process step 410). Switch 111 repeats steps 405 and 410 N times, once per time slot (process step 415). Next, switch 111 finds a maximal matching of inputs and outputs over all active cells currently queued at the internal input buffers of the CIOQ (process step 420). Switch 111 then configures bufferless crossbar 340 according to the current matching (process step 425) and transmits the matched head of line (HOL) cell at each VOQ (process step 430). Switch 111 then repeats step 420, 425 and 430 2N times, twice per time slot (i.e., speed-up of two) (process step 435). [Emphasis Added]

It is respectfully submitted that this amendment does not introduce any new matter, and it's entry is requested.

The bufferless, non-blocking interconnecting network is a configurable component that receives "from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate."

The Office Action has asserted that this bufferless, non-blocking interconnecting network is rendered obvious by element 89 of Krishna. Applicant respectfully disagrees. For the purpose of clarity, the relevant portion of Figure 14 of Krishna is reproduced below:



As shown above, element 89 of Krishna is simply a series of connections. It is not connected to a controller, nor is it configurable by a controller. In contrast, claim 1, comprises the elements "a bufferless, non-blocking interconnecting network to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate" and "wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network".

Figure 3 of the present disclosure, which is reproduced below, illustrates the connections of the bufferless, non-blocking interconnecting network to the scheduling controller:

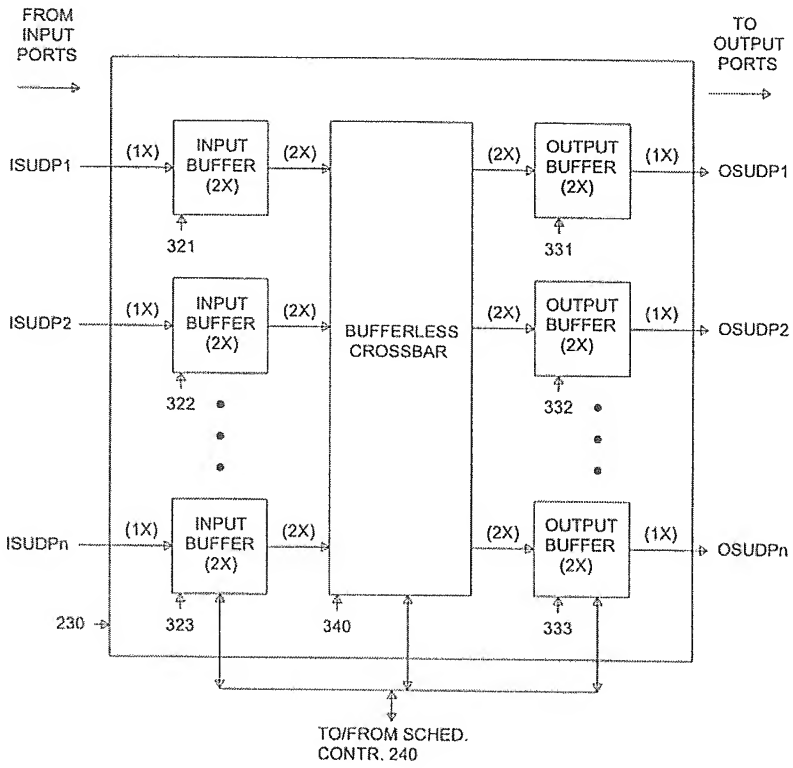


FIGURE 3

As shown by one embodiment of the present disclosure, the configurable bufferless, non-blocking interconnecting network of Claim 1 is illustrated in Figure 3 as bufferless crossbar 340. Element 89 of Krishna is neither connected to a schedule controller, nor is it configurable. It is therefore respectfully submitted that the configurable bufferless, non-blocking interconnecting network of Claim 1 is not anticipated, taught, or suggested by Krishna.

Krishna therefore fails to teach a *bufferless, non-blocking interconnection network*, as required by Claim 1 and its dependents, Claims 2 and 3. Similar arguments are true for Claim 4 (and its dependents, Claims 5 and 6), Claim 7 (and its dependents, Claims 8-13) and Claim 14 (and its dependents Claims 15-20)

Moreover, there is no suggestion or motivation within *Krishna* to prompt one of ordinary skill to selectively combine discrete elements from *Krishna* and then *seek out* still others as required by the claims of the present application.

Accordingly, the Applicant respectfully requests favorable reconsideration and the withdrawal of the §103 rejection.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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